CLAIMS:

What is claimed is:

1. A memory driver comprising:

selection logic, to receive an address for promotion to a memory, and to provide an indication of whether to promote the received address or a modified version thereof to the memory; and

a multiplexing element, responsive to the selection logic, to selectively promote either the received address or the modified version thereof to the memory based, at least in part, on the received indication.

2. A memory driver according to claim 1, further comprising:

a latch element, coupled to the multiplexing element, to assert address content received from the multiplexing element to the memory.

3. A memory driver according to claim 2, the latch element comprising:

a pulse generator element, to receive a clock signal and produce at least two reference signals, overlapping yet offset from one another in time; and

one or more driver elements, coupled to the multiplexing element and responsive to the pulse generator element, to receive content promoted from the multiplexing element during a precharge phase the reference signals, and to assert the content received from the multiplexer to the memory during a discharge phase of the reference signals.

4. A memory driver according to claim 3, the pulse generator element comprising:

two parallel processing paths, one of which including a delay element, wherein the parallel processing paths receive the clocking signal, or a delayed version thereof, at a gate of a transistor to control the precharge and discharge cycles of the coupled latch.

5. A memory driver according to claim 3, the driver element comprising:

a differential domino transistor architecture, coupled to the multiplexer output and responsive to the pulse generator, to generate a differential memory output of an element of the promoted address content and its complement.

6. A memory driver according to claim 1, the selection logic comprising:

detection logic, to determine whether at least a subset of the received address is composed of zeroes.

7. A memory driver according to claim 6, wherein the detection logic is a one-detect circuit.

8. A memory driver according to claim 1, the selection logic comprising:

detection logic, to determine whether at least a subset of the received address is composed of a predefined value.

9. A memory driver according to claim 1, the multiplexer element comprising:

a first and second set of stacked transistors, wherein individual transistors of the first set are coupled to receive at their gate one of an indication from the selection logic, an address, and

a process identification (PID) value, while individual transistors of the second set are coupled to receive at their gate a complement of the indication, the address and the PID value.

10. A memory driver according to claim 9, wherein depending on the indication received from the selection logic, the multiplexer element promotes either the received address and complement thereof, or the process identifier (PID) and complement thereof to the latch element.

11. A memory driver according to claim 1, the latch comprising:

a first and second differential set of transistors, coupled to the multiplexing element, to assert either the received address and complement thereof, or the PID and complement thereof to a memory device.

12. A memory driver according to claim 11, wherein the latch is coupled to the multiplexing element through a transistor responsive to a pulse generator, such that the latch is isolated from the multiplexing element during a precharge phase of the pulse generator, and asserts content at the output of the multiplexing element during a discharge phase of the pulse generator.

13. A system comprising:

a content addressable memory (CAM); and

a memory driver, coupled with the CAM, to receive an address for assertion to the CAM, and to selectively modify the at least a subset of the received address to reflect a process identifier based, at least in part, on at least a subset of content of the received address.

14. A system according to claim 13, the memory driver comprising:

selection logic, to receive the address for promotion to a CAM cell, and to provide an indication of whether to promote the received address or a modified version thereof to the CAM cell; and

a multiplexing element, responsive to the selection logic, to selectively promote either the received address or the modified version thereof to the CAM cell based, at least in part, on the received indication.

15. A system according to claim 14, the memory driver further comprising:

a latch element, coupled to the multiplexing element, to assert address content received from the multiplexing element to the memory cell.

16. A method implemented within a memory driver comprising:

receiving at least a subset of an address for promotion to a memory; and

selectively replacing at least the subset of the received address with a process identifier (PID) if it is determined that the subset of the received addresses is composed of zeroes.

17. A method implemented within a memory driver according to claim 16, further comprising:

analyzing the received subset of the address to determine whether the subset of composed of zeroes and, if so, to provide an indication to a multiplexing element to replace the received subset of the address with the process identifier.

18. A method implemented within a memory driver according to claim 18, further comprising:

asserting either the received address, or a modified version thereof based, at least in part, on whether the received subset of the address is composed of zeroes.

19. A storage medium comprising content, which when executed by an accessing machine, causes the machine to implement a method according to claim 16.

20. A storage medium comprising content which, when executed by an accessing machine, causes the machine to generate a memory driver according to claim 1.